AMENDMENTS TO THE SPECIFICATION

Please amend paragraph 4 of the application as follows:

[0004] The need for integrating fast, flexible, inexpensive memory into these logic products to provide memory for a variety of purposes such as register files, FIFOs, scratch pads, look-up tables, etc. has become more apparent, because there are significant cost and performance savings to be obtained by integrating this functionality directly into, for example, an FPGA. However, providing this memory by having something other than explicitly dedicated SRAM blocks included in the FPGA has not proved satisfactory. Typically, the implementation of memory without dedicated SRAM blocks in an FPGA has been done by either providing external SRAM to the FPGA or by using the logic modules, flip-flops and interconnect of the FPGA. Both of these solutions are less than satisfactory.

Please amend paragraph 34 as follows:

[0034] Turning now to FIG. 3, a block diagram of the FPGA core 10 in a flexible, high-performance SRAM based FPGA architecture having user-assignable SRAM blocks 12 according to the present invention is illustrated. The FPGA core 10 includes a plurality of logic function modules disposed within a multi-level architecture (MLA) of routing resources. The blocks 14-1 through 14-4 in FPGA core 10 illustrate a grouping of logic modules in the MLA termed MLA4. In the preferred embodiment, there are approximately 50K gates combined in blocks 14-1 through 14-4. The SRAM blocks 12 comprise 16K bits of user-assignable SRAM divided into eight dedicated blocks of 2K bits. The user-assignable SRAM blocks 12 will be more fully described below.

Please amend paragraph 42 as follows:

[0042] Referring now to ~~PIG~~. FIG. 7, a more detailed block diagram of a portion of the FPGA core 10 depicts the interconnectivity between the SRAM block bus architecture and the routing channels of an MLA3 32. In FIG. 7, connectors 34 between an MLA3 32 and the SRAM blocks 12 are disposed on the edge of an MLA3 32 adjacent an SRAM block 12. Each of the connectors 34 represents a plurality of user-programmable interconnect elements disposed between the conductors of a routing channel in an MLA3 32 and a plurality of pass-through interconnect conductors 36 spanning the SRAM block 12.